Low Drop Out regulators:

basic principles

and

design examples

Prof Lorenzo Capineri

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Topics

- Basic theory of LDO
- Analysis of technical characteristics of TPS749xx (TI) device
- Design of a power supply system for an analog-digital processing board

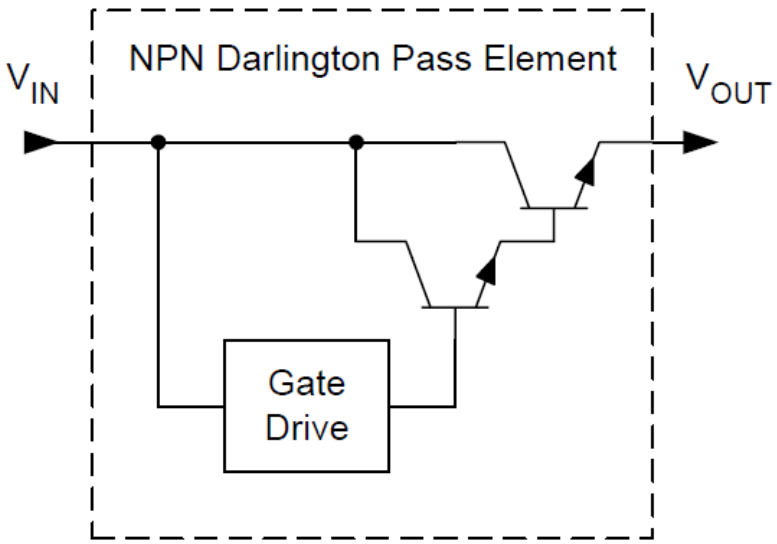
LDO: Low Dropout regulator

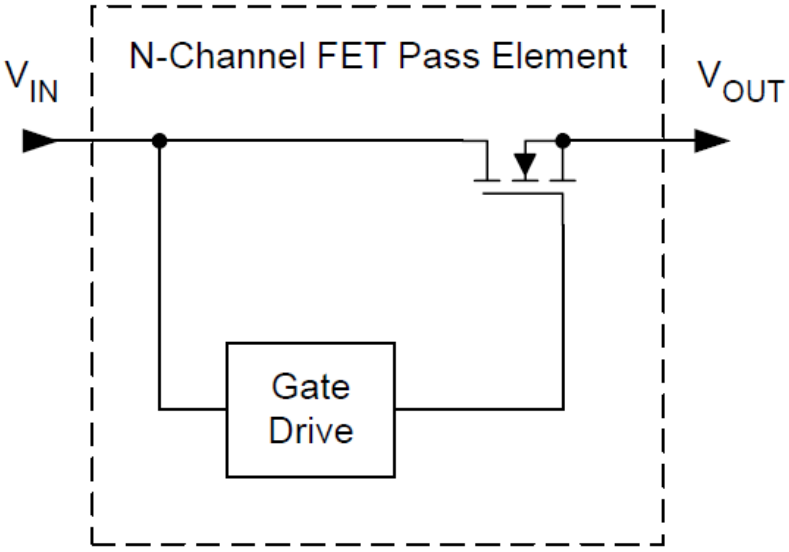
Low dropout regulators (LDOs) are linear (dissipative) regulators. They are a simple inexpensive way to regulate an output voltage that is powered from a higher voltage input. They are easy to design with and use. For most applications, the parameters in an LDO datasheet are usually very clear and easy to understand.

However, other applications require the designer to examine the datasheet more closely to determine whether or not the LDO is suitable for the specific circuit conditions.

The main advantage (and difference) from 3 or 4 terminal linear regulators with power BJT pass element is the operation with small drop out voltage within a load current limit.

Standard Regulators and LDOs

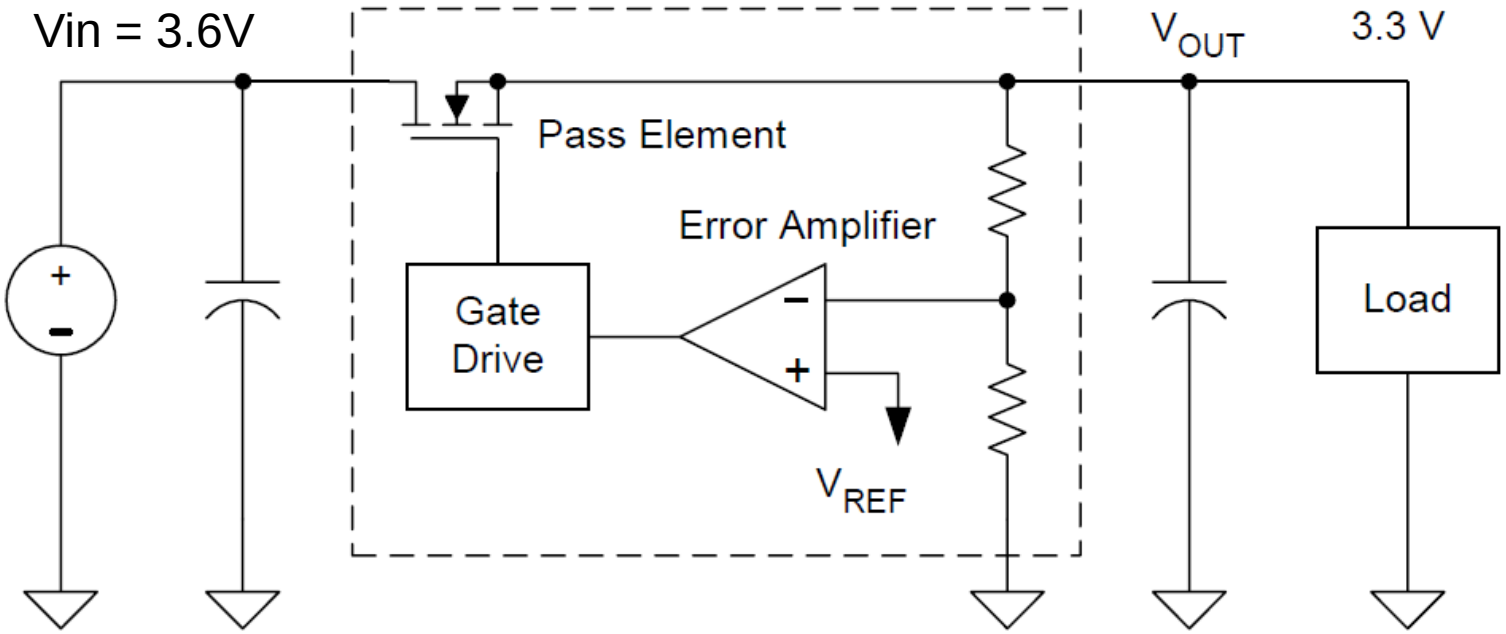




Darlington configuration needs to operate with high Vce in the linear region because the summation of the two V_{BE}'s.

Standard linear regulators have voltage drops as high as 2 V which are acceptable for applications with large input-to-output voltage difference such as generating 2.5 V from a 5 V input.

LDO block diagram



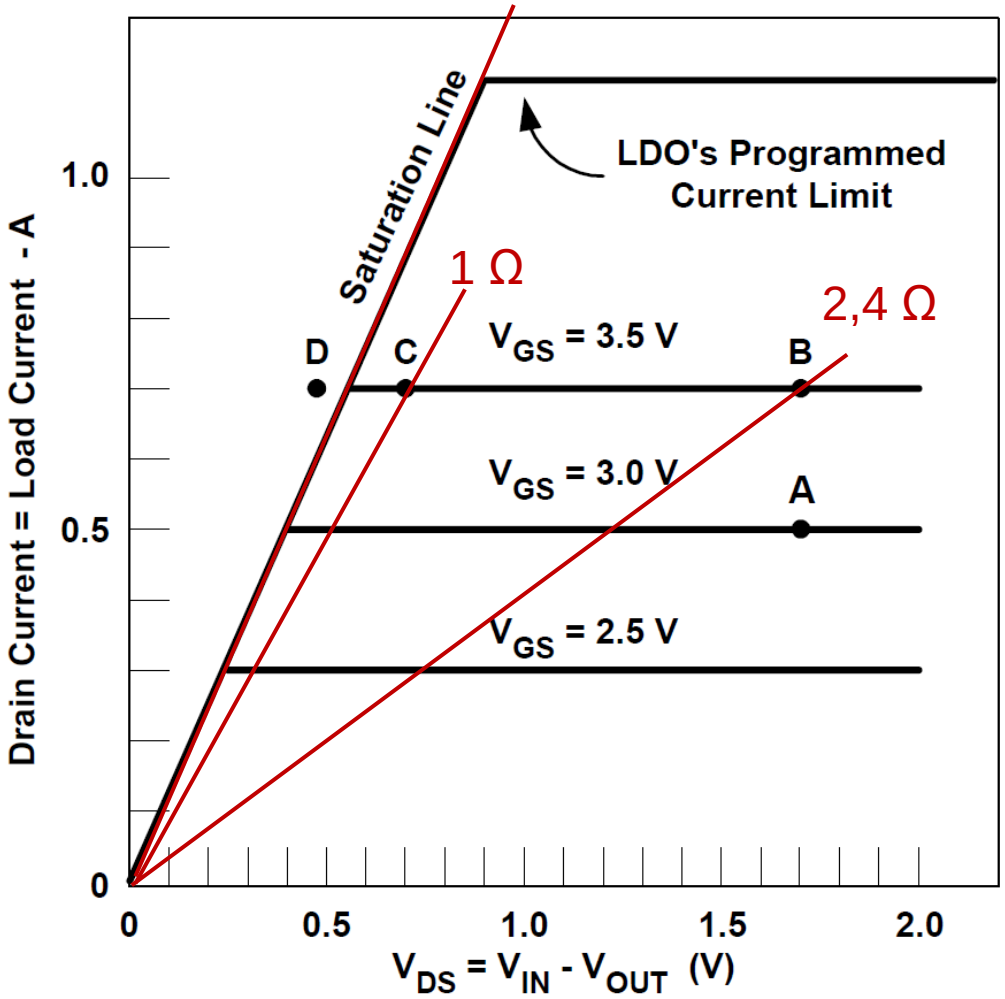
The power Mosfet works as series pass element and regulates the output voltage by the R_{dsON}.

Power Mosfet operating in saturation has very low value of R_{dsON} and so the small drop out voltages → Vin close to Vout can be regulated efficiently.

Example: Vout = 3.3 V with Vin = 3.6V Li-Ion battery requires the operation with only 300 mV of drop out voltage and good efficiency!!

Operating region of an LDO's N- channel pass element

Drop Out region with minimum Rds(ON) = 0,8 Ω



Rated drop out voltage

Data sheets provide the maximum $V_{DROPOUT}$ for a rated output current (I_{OUT}) at nominal V_{OUT} in a specified temperature range :

$$V_{DROPOUT} = I_{OUT} \times R_{dsON}$$

- Depending on the rated output current, R_{dsON} goes from 0,1 Ω to 10 Ω and with output current from 0.1 – 0.5 A.
- R_{dsON} values depends on die size and package type.
- Typically line voltage regulation coefficient are very small also for low output voltages as low as 1.2 V.

LDO noise

$$PSRR = 20 \times \log\left(\frac{V_{IN\_ripple}}{V_{OUT\_ripple}}\right).$$

Figure 1. Plot of linear regulator's wide-bandwidth, high PSRR

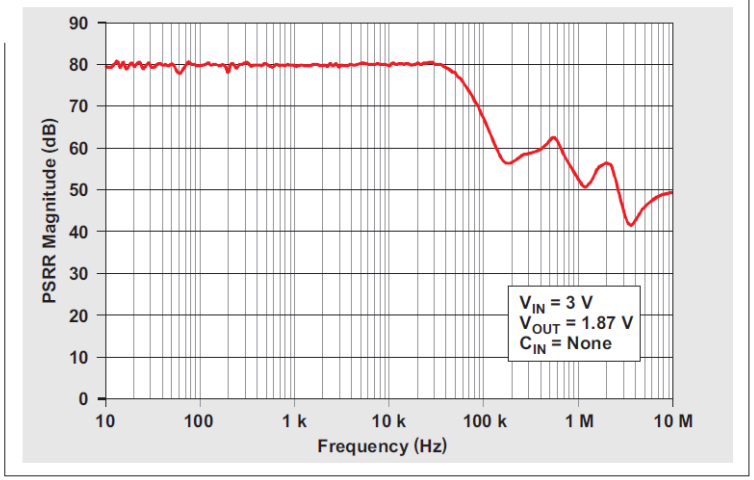


Figure 2. Typical noise spectrum from a switching regulator

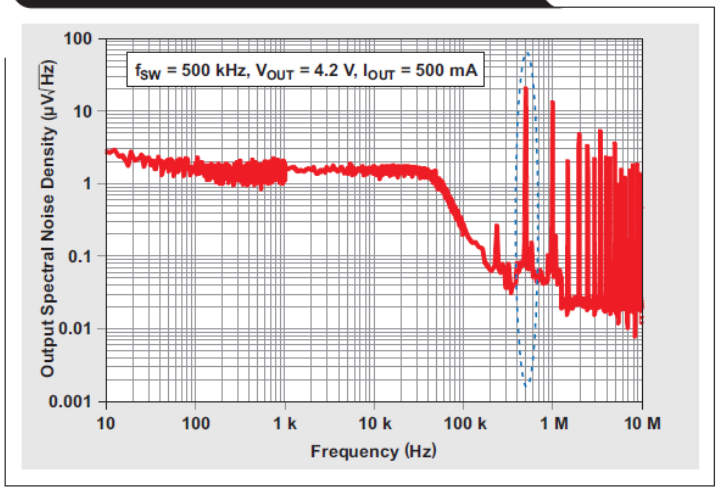
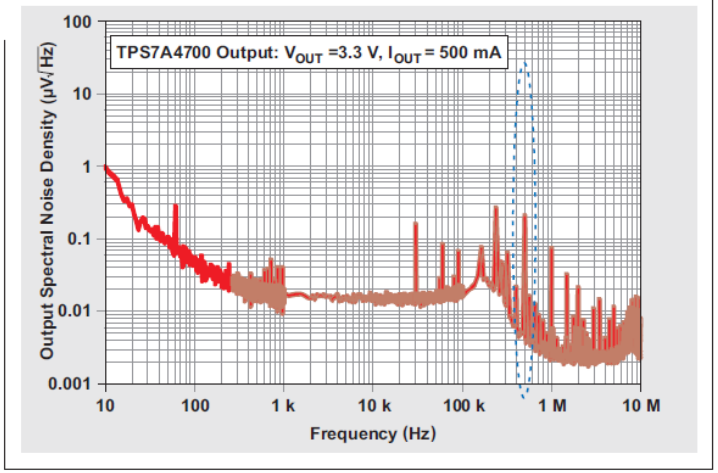


Figure 3. Output noise spectrum of TPS7A4700 linear regulator with attenuated 500-kHz spike



Vin

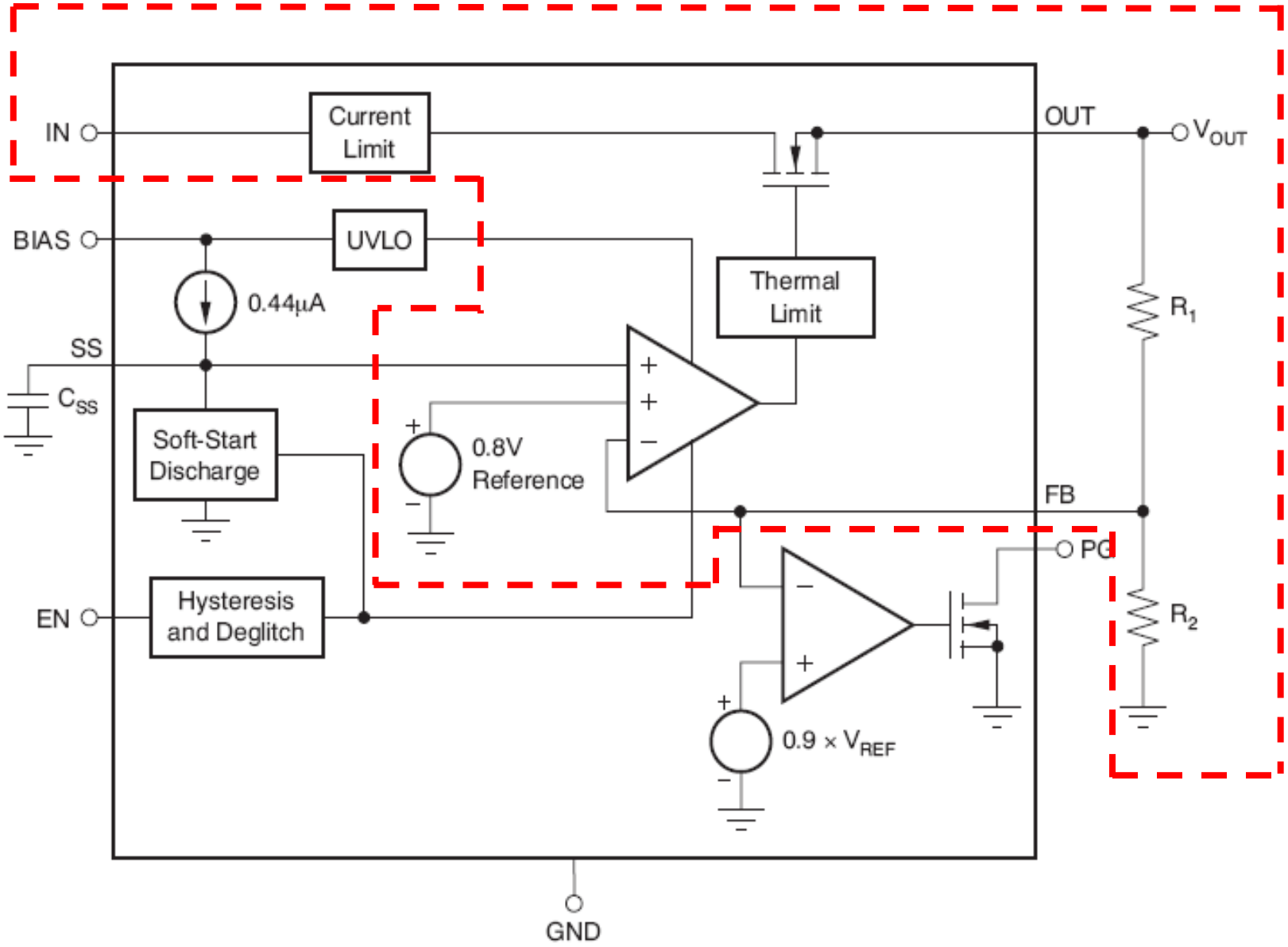
Switching regulator

4,2V

LDO regulator

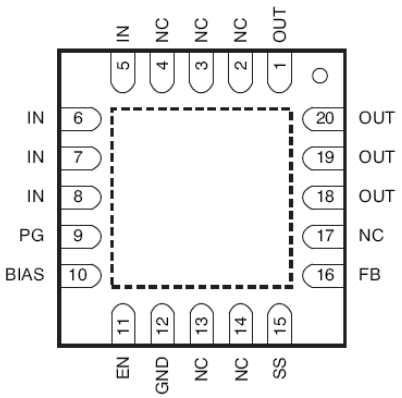
3,3V

Block diagram of device TPS74901

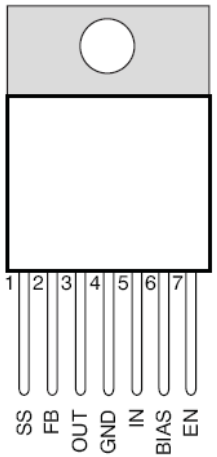


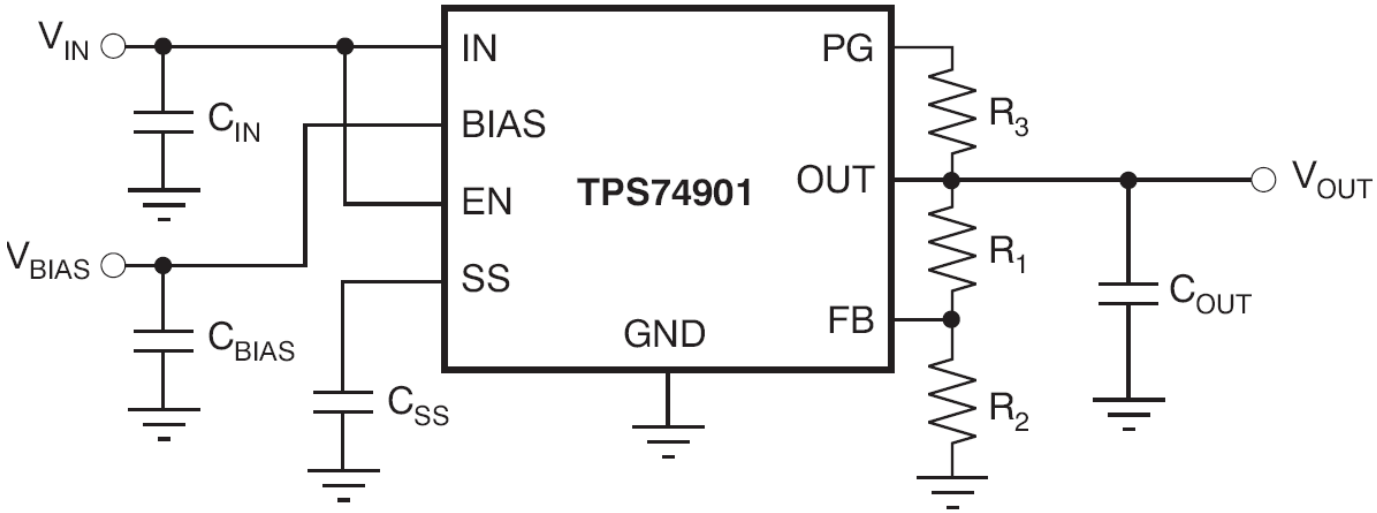
Variable output voltage with TPS74901

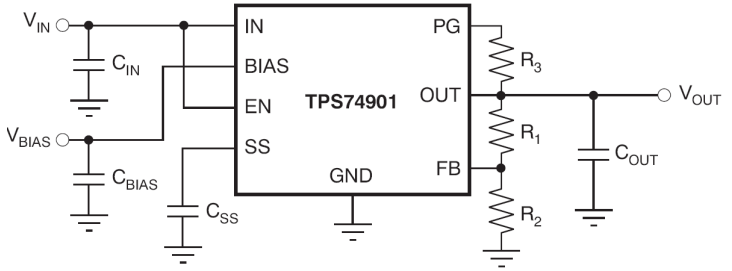
RGW PACKAGE
QFN-20
(TOP VIEW)



KTW PACKAGE
DDPAK-7
(TOP VIEW)







- ***IN*** Input voltage
- ***BIAS*** Reference voltage and internal circuit supply voltage.
- ***EN (ENABLE)*** Enable active positive
- ***SS (SOFT START)*** With external capacitor the start-up time can be controlled. Otherwise the default start-up time is100µs
- ***PG (POWER GOOD)*** Indicates when the output voltages is above a defined threshold (typivally 90% of the nominal output voltage) and the device is fully operating.
- ***OUT*** Regulated output voltage
- ***FB (FEEDBACK)*** voltage feed back input
- ***GND***
- ***NC***
- ***PAD/TAB*** Thermal PAD to be soldered to ground plane of PCB to dissipate thermal power.

ELECTRICAL CHARACTERISTICS

At T_J = –40°C to +125°C, V_{EN} = 1.1V, V_{IN} = V_{OUT} + 0.3V, C_{BIAS} = 0.1µF, C_{IN} = C_{OUT} = 10µF, C_{NR} = 1nF, I_{OUT} = 50mA, and V_{BIAS} = 5.0V, unless otherwise noted. Typical values are at T_J = +25°C.

PARAMETER		TEST CONDITIONS	TPS74901 MIN	TPS74901 TYP	TPS74901 MAX	UNIT
V_{IN}	Input voltage range		V_{OUT} + V_{DO}		5.5	V
V_{BIAS}	Bias pin voltage range		2.7		5.5	V
V_{REF}	Internal reference (Adj.)	T_J = +25°C	0.798	0.802	0.806	V
V_{OUT}	Output voltage range	V_{IN} = 5V, I_{OUT} = 3.0V	V_{REF}		3.6	V
	Accuracy (RGW package)(1)	V_{OUT} + 2.2V ≤ V_{BIAS} ≤ 5.5V, 50mA ≤ I_{OUT} ≤ 3.0A	–2	±0.5	2	%
	Accuracy (KTW package)(1)	V_{OUT} + 2.4V ≤ V_{BIAS} ≤ 5.5V, 50mA ≤ I_{OUT} ≤ 3.0A	–2	±0.5	2	%
V_{OUT}/V_{IN}	Line regulation	$V_{OUT\ (NOM)}$ + 0.3 ≤ V_{IN} ≤ 5.5V		0.03		%/V
V_{OUT}/I_{OUT}	Load regulation	50mA ≤ I_{OUT} ≤ 3.0A		0.09		%/A
V_{DO}	V_{IN} dropout voltage(2)	I_{OUT} = 3.0A, $V_{BIAS} - V_{OUT\ (NOM)} \geq 3.25V$(3)		120	280	mV
	V_{BIAS} dropout voltage(2)	I_{OUT} = 3.0A, V_{IN} = V_{BIAS}		1.31	1.75	V
I_{CL}	Current limit	V_{OUT} = 80% × $V_{OUT\ (NOM)}$, RGW Package	3.9	4.6	5.5	A
		V_{OUT} = 80% × $V_{OUT\ (NOM)}$, KTW Package	3.8	4.6	5.5	
I_{BIAS}	Bias pin current			1	2	mA

I_{SHDN}	Shutdown supply current (I_{GND})	$V_{EN} \le 0.4V$		1	50	µA
I_{FB}	Feedback pin current		–1	0.150	1	µA
PSRR	Power-supply rejection (V_{IN} to V_{OUT})	1kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V		60		dB
		300kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V		30		
	Power-supply rejection (V_{BIAS} to V_{OUT})	1kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V		50		dB
		300kHz, I_{OUT} = 1.5A, V_{IN} = 1.8V, V_{OUT} = 1.5V		30		
Noise	Output noise voltage	100Hz to 100kHz, I_{OUT} = 3.0A, C_{SS} = 0.001µF		25 × V_{OUT}		μV_{RMS}
t_{STR}	Minimum startup time	R_{LOAD} for I_{OUT} = 1.0A, C_{SS} = open		200		µs
I_{SS}	Soft-start charging current	V_{SS} = 0.4V		440		nA
$V_{EN, HI}$	Enable input high level		1.1		5.5	V
$V_{EN, LO}$	Enable input low level		0		0.4	V
$V_{EN, HYS}$	Enable pin hysteresis			50		mV
$V_{EN, DG}$	Enable pin deglitch time			20		µs
I_{EN}	Enable pin current	V_{EN} = 5V		0.1	1	µA
V_{IT}	PG trip threshold	V_{OUT} decreasing	85	90	94	$\%V_{OUT}$
V_{HYS}	PG trip hysteresis			3		$\%V_{OUT}$
$V_{PG, LO}$	PG output low voltage	I_{PG} = 1mA (sinking), $V_{OUT} < V_{IT}$			0.3	V
$I_{PG, LKG}$	PG leakage current	V_{PG} = 5.25V, $V_{OUT} > V_{IT}$		0.1	1	µA
T_J	Operating junction temperature		–40		+125	°C
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		+165		°C
		Reset, temperature decreasing		+140		

SOFT START PROGRAMMABILE (SS)

soft start time: Css defines a suitable value of start time when LDOs provide power supply to digital board (FPGA, DSP...) that need to be initialised.

$$t_{SS}(s) = 0.8 \times C_{SS}(F)/7.5 \times 10^{-7}$$

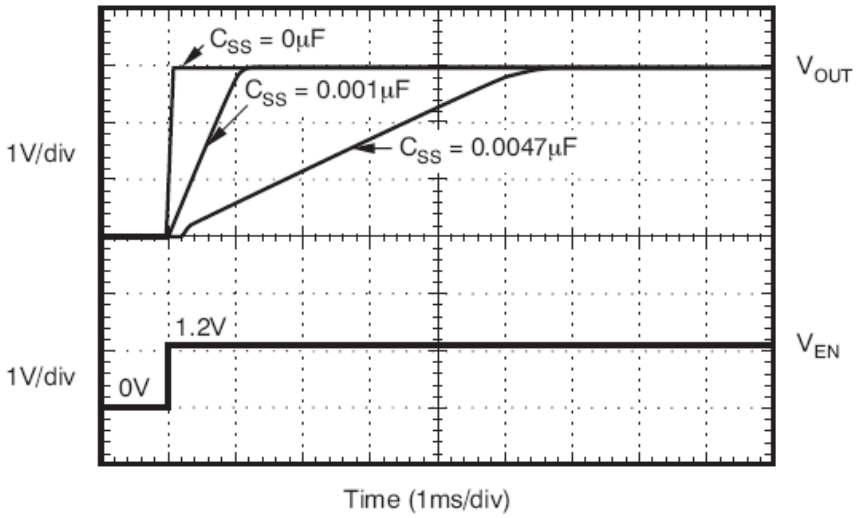


Table 2. Standard Capacitor Values for Programming the Soft-Start Time(1)

C_{SS}	SOFT-START TIME
Open	0.1ms
470pF	0.5ms
1000pF	1ms
4700pF	5ms
0.01µF	10ms
0.015µF	16ms

Default start-up is 100µs

Vout setting with feedback resistor R1 and R2

Table 1. Standard 1% Resistor Values for Programming the Output Voltage(1)

R_1 (kΩ)	R_2 (kΩ)	V_{OUT} (V)
Short	Open	0.8
0.619	4.99	0.9
1.13	4.53	1.0
1.37	4.42	1.05
1.87	4.99	1.1
2.49	4.99	1.2
4.12	4.75	1.5
3.57	2.87	1.8
3.57	1.69	2.5
3.57	1.15	3.3

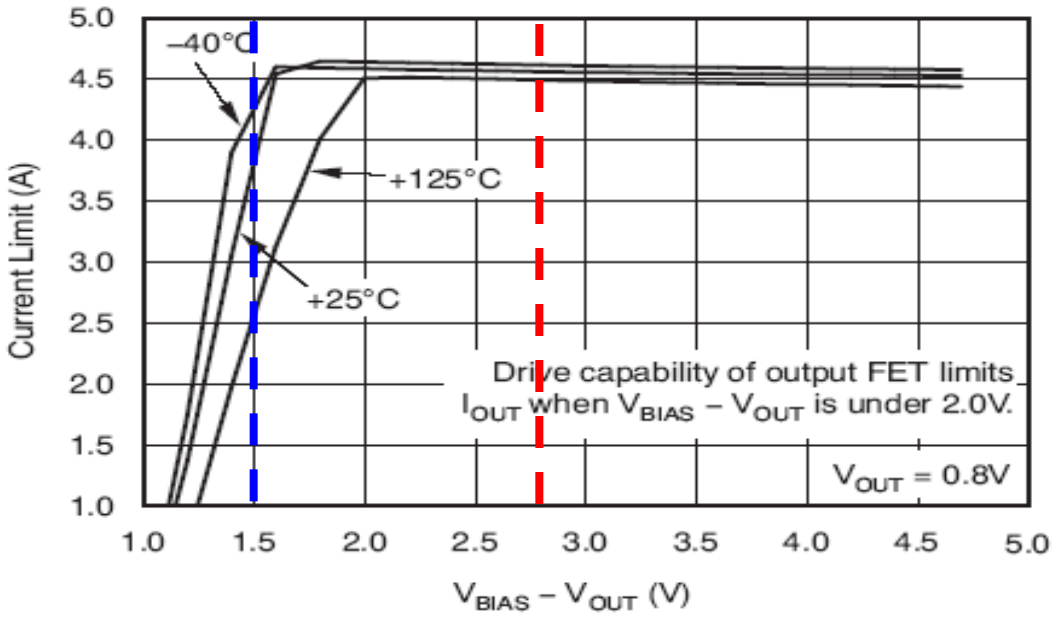
Per avere la maggiore accuratezza possibile R2 dovrebbe essere ≤ 4.99kΩ

$$V_{OUT} = 0.8 \times (1 + R_1/R_2)$$

C_{IN}, C_{BIAS} , C_{OUT}

- $C_{OUT} \geq 2.2\mu F$
- C_{IN} and $C_{BIAS} \geq 1\mu F$. If Vin and Vbias are connected to the same voltage source $C_{BIAS} \geq 4.7\mu F$
- Ceramic capacitors with low ESR need to be mounted as close as possible to device pins.

Output Current limitation



Case 1

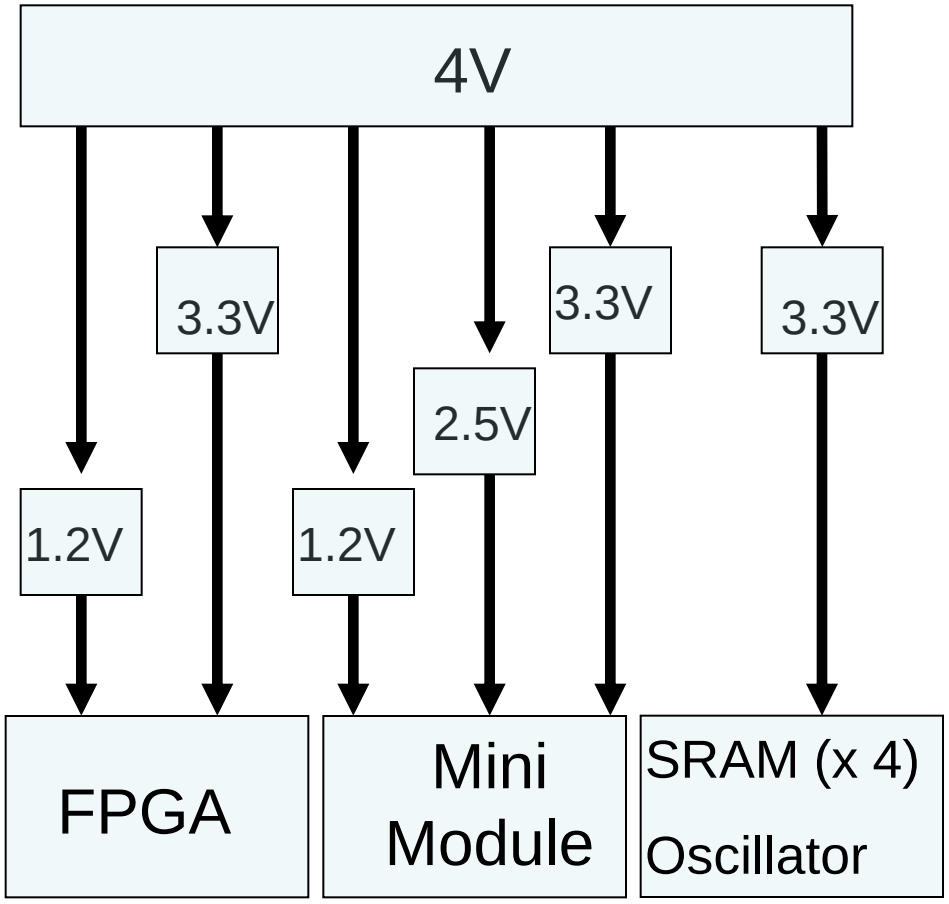
- V_{BIAS}=4V
- V_{OUT}=1.2V
- $V_{BIAS} - V_{OUT}$ = 2.8V

Case 2

- V_{BIAS}=4V
- V_{OUT}=2.5V
- $V_{BIAS} - V_{OUT}$ = 1.5V

Note: with low ($V_{BIAS} - V_{OUT}$) the current limit is temperature dependent !

Example of Power Supply for a digital board (Prima project)



- Primary voltage source is chosen +4V from a switching regulator and different outputs for the digital components are provided.
- The board host high sensitivity sensors for radiation detection: low noise power supply is required LDO

Power supply specifications

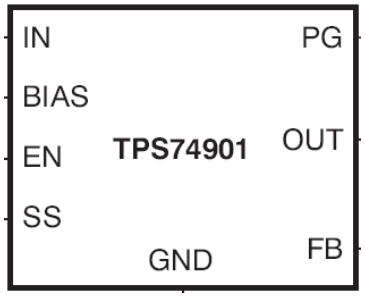
DISPOSITIVO	CORRENTE STAND BY	CORRENTE ATTIVA
FPGA	175mA	3.6A
MiniModule	445mA	6A
Memoria	200mA	1.1A
Oscillatore	Sempre attivo	40mA

Load currents

DISPOSITIVO	POTENZA DISSIPATA STAND BY	POTENZA (max) DISSIPATA ATTIVA
FPGA	0.53W	8.73W
MiniModule	1.07W	14W
Memoria	0.66W	3.63W
Oscillatore	Sempre attivo	0.132W

Power dissipation

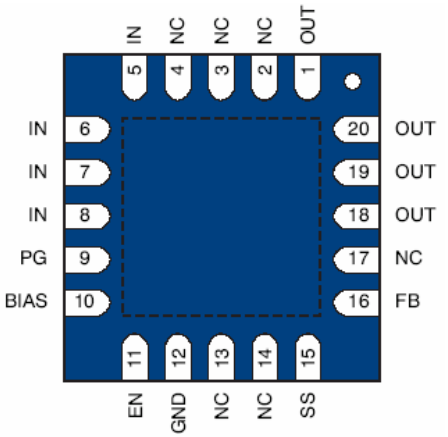
LDO Vout=1.2V TPS74901RGWT



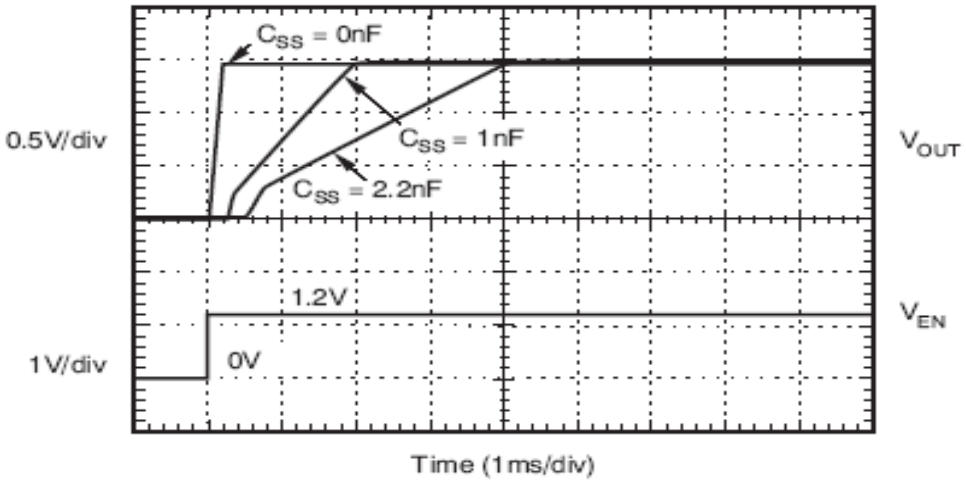
- Reference voltage 1.2V set by external feed back resistors

- Max Output current 3A

- EN enable pin handled

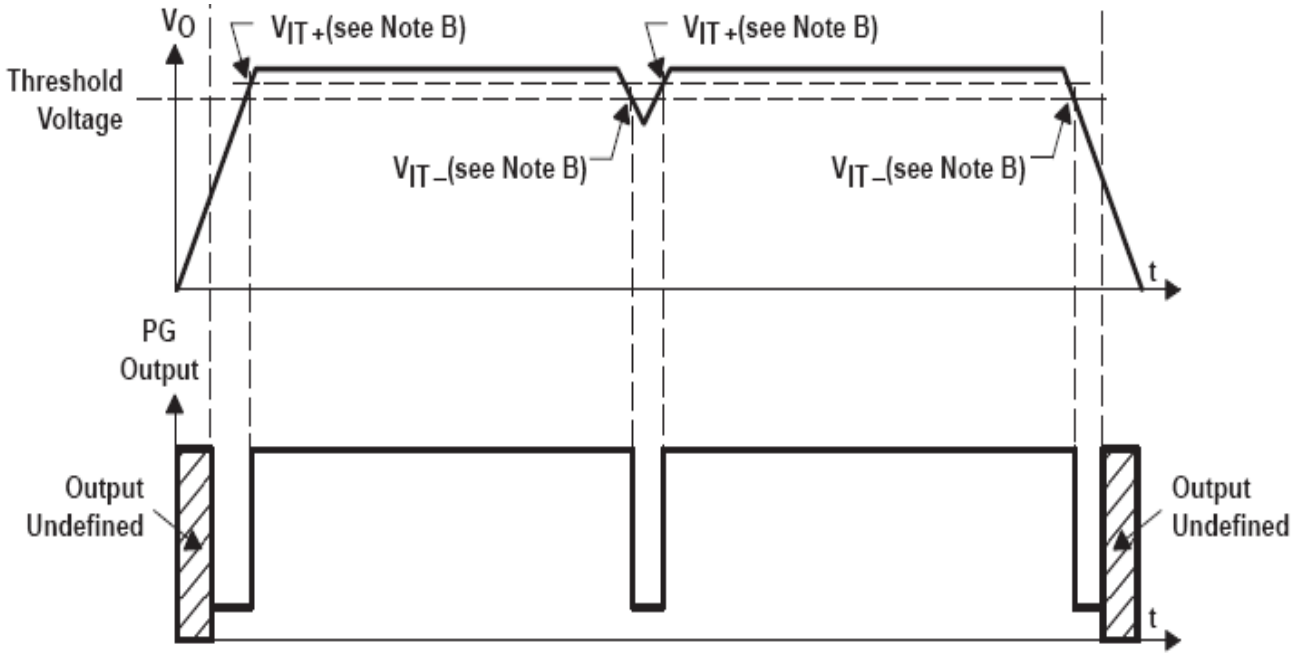


RGW Package
QFN-20 (top view)



- SS “soft start”, C_{SS} = 1nF to delay of about 2 ms

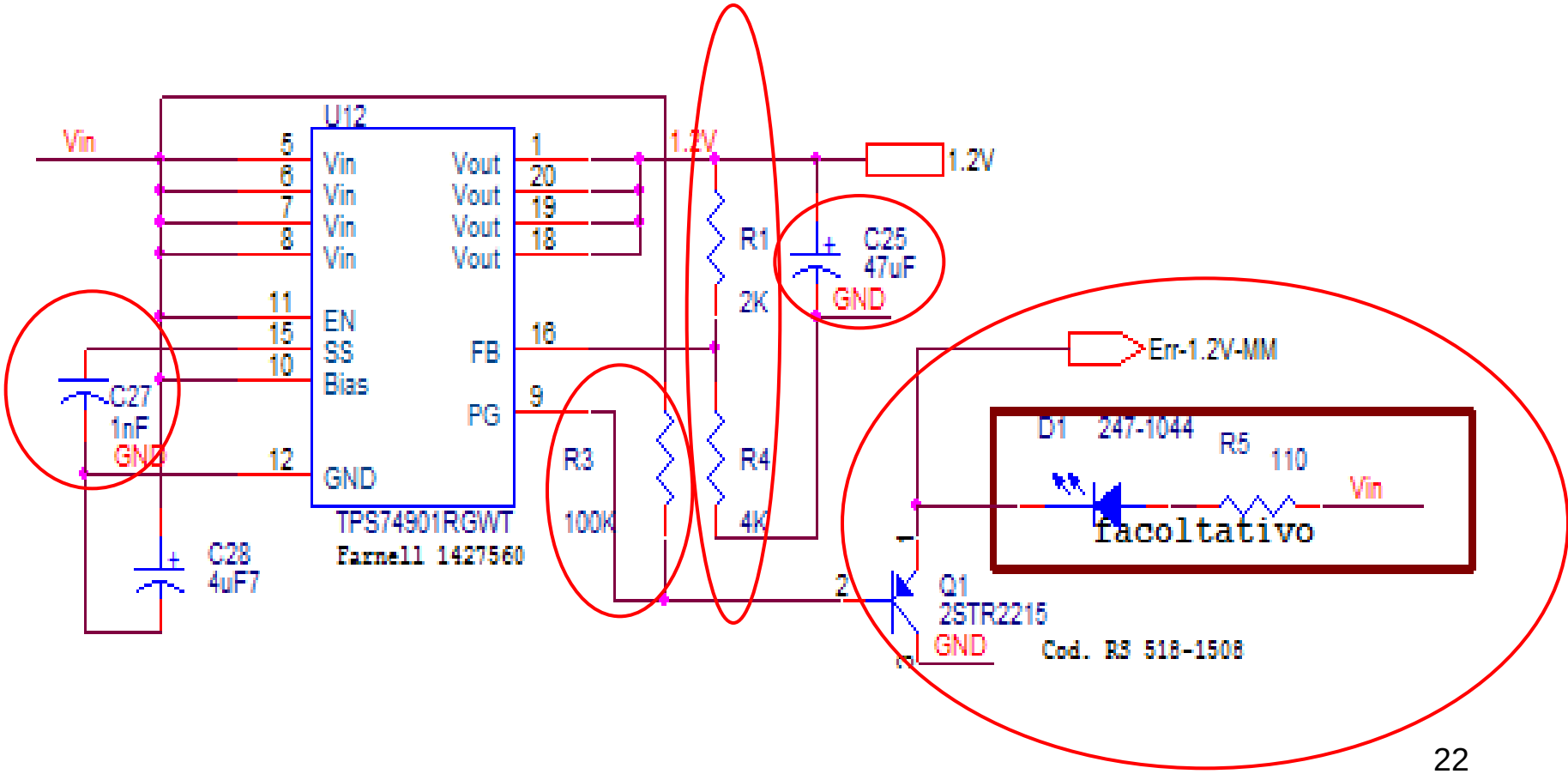
LDO Vout=1.2V TPS74901RGWT



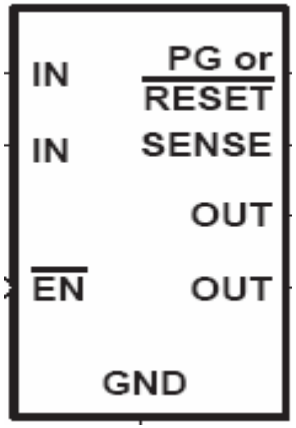
- PG Vout monitoring, goes to low impedance if an error is detected on output voltage regulation. Power diagnostic firmware handles this pin output.

LDO Vout=1.2V TPS74901RGWT

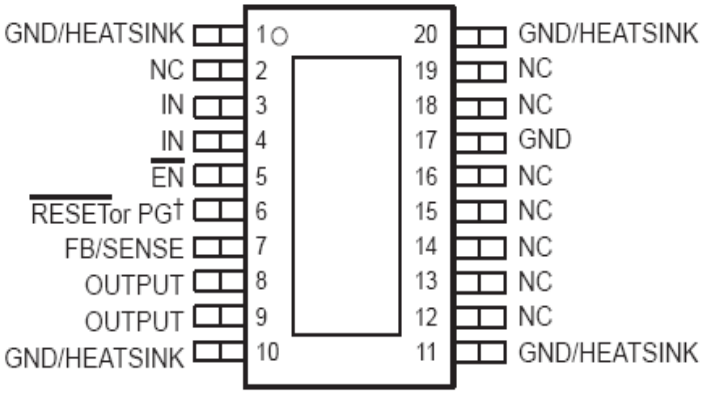
Schematic.

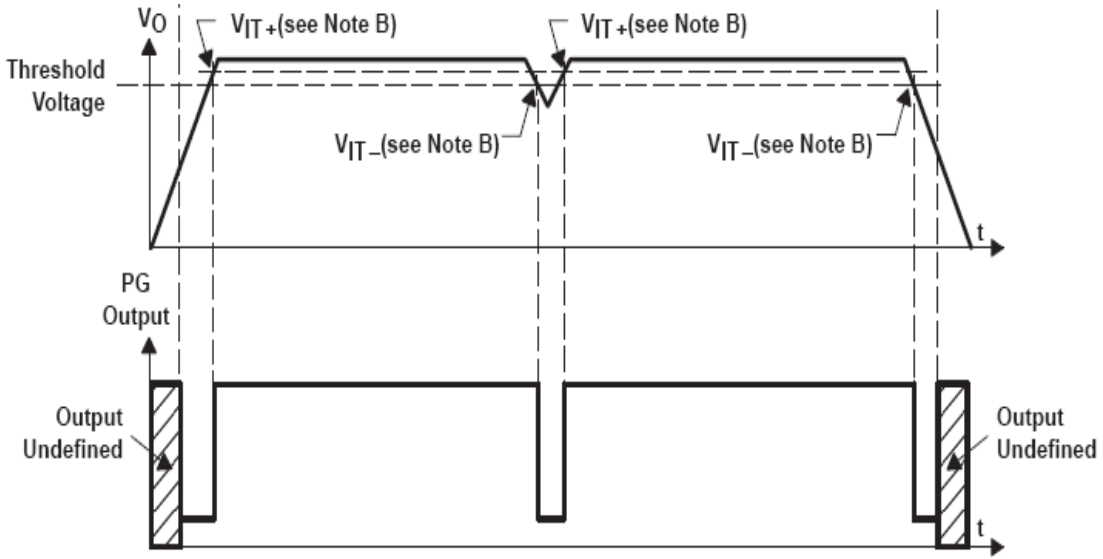


LDO Vout = 2.5V TPS75225QPWP



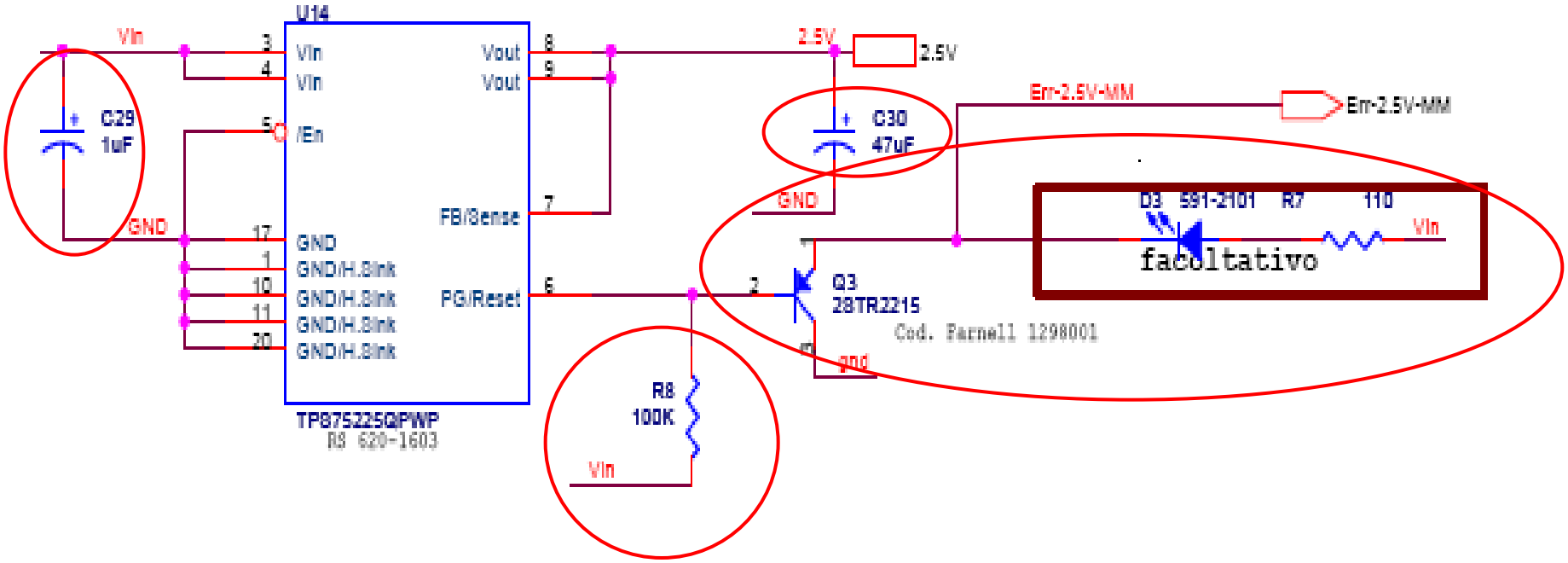
- Output voltage 2.5V
- Max Output Current 2A
- Package TSSOP (QPWP) 20 pin
- PG output handled
- /EN pin



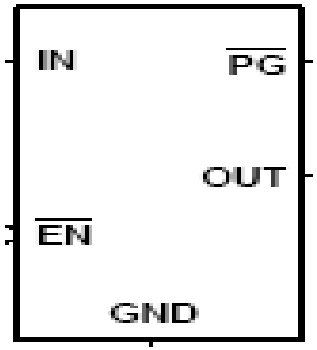


LDO Vout =2.5V TPS75225QPWP

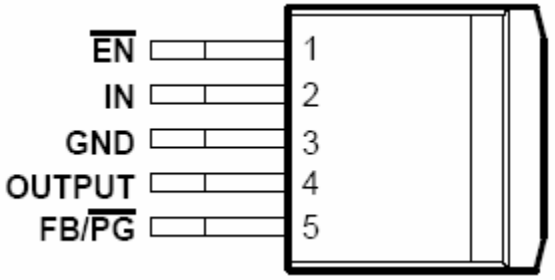
Schematic.

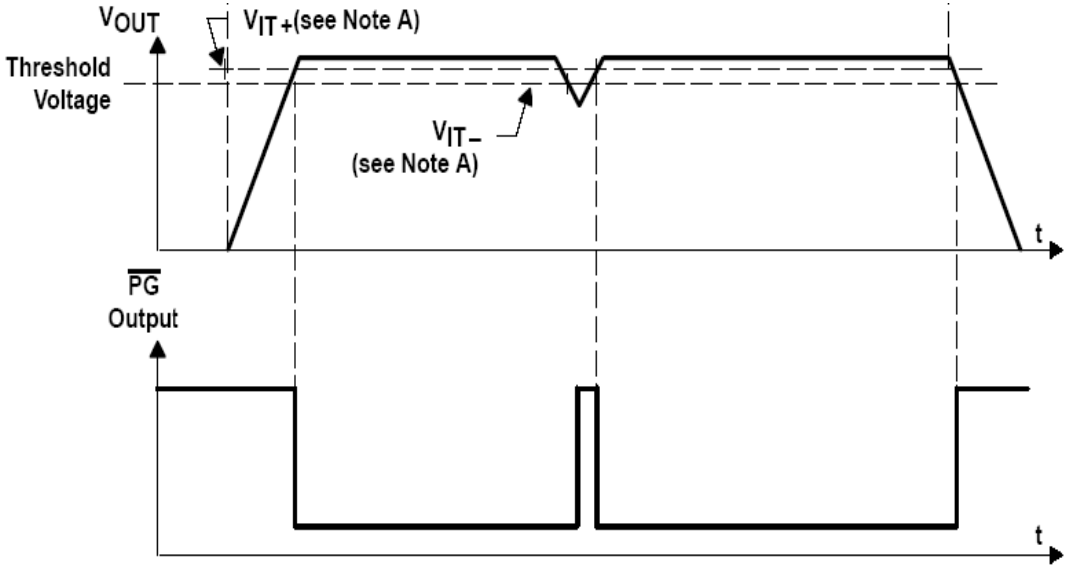


LDO Vout = 3.3V TPS75733KC



- Output voltage 3.3V
- Current output 3A
- Package TO-263 KTT
- PG handled
- /EN

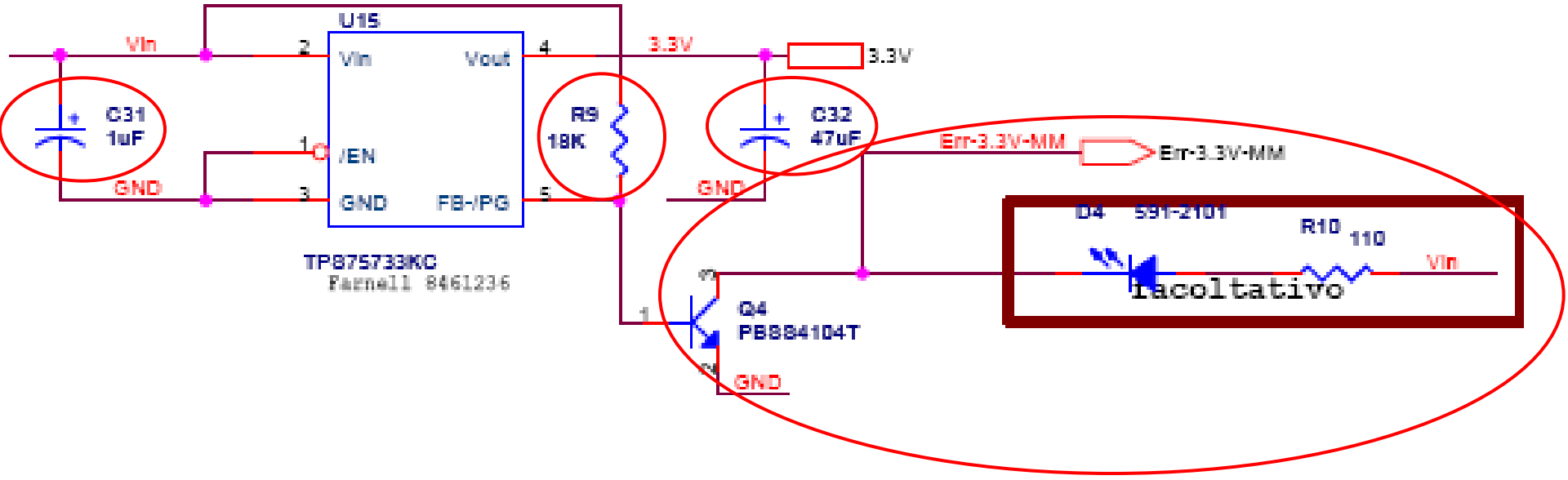




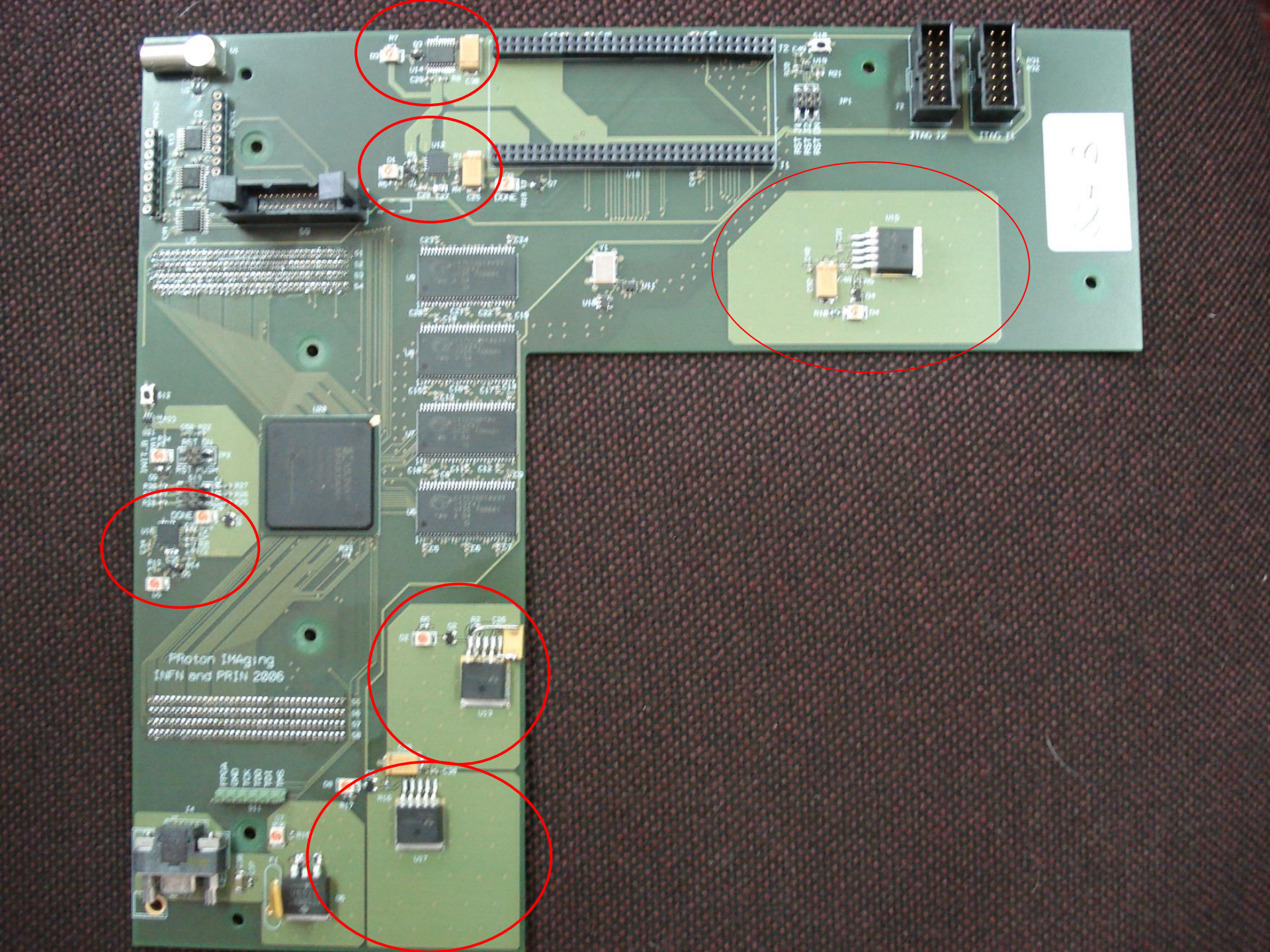
LDO Vout= 3.3V TPS75733KC

Schematic.

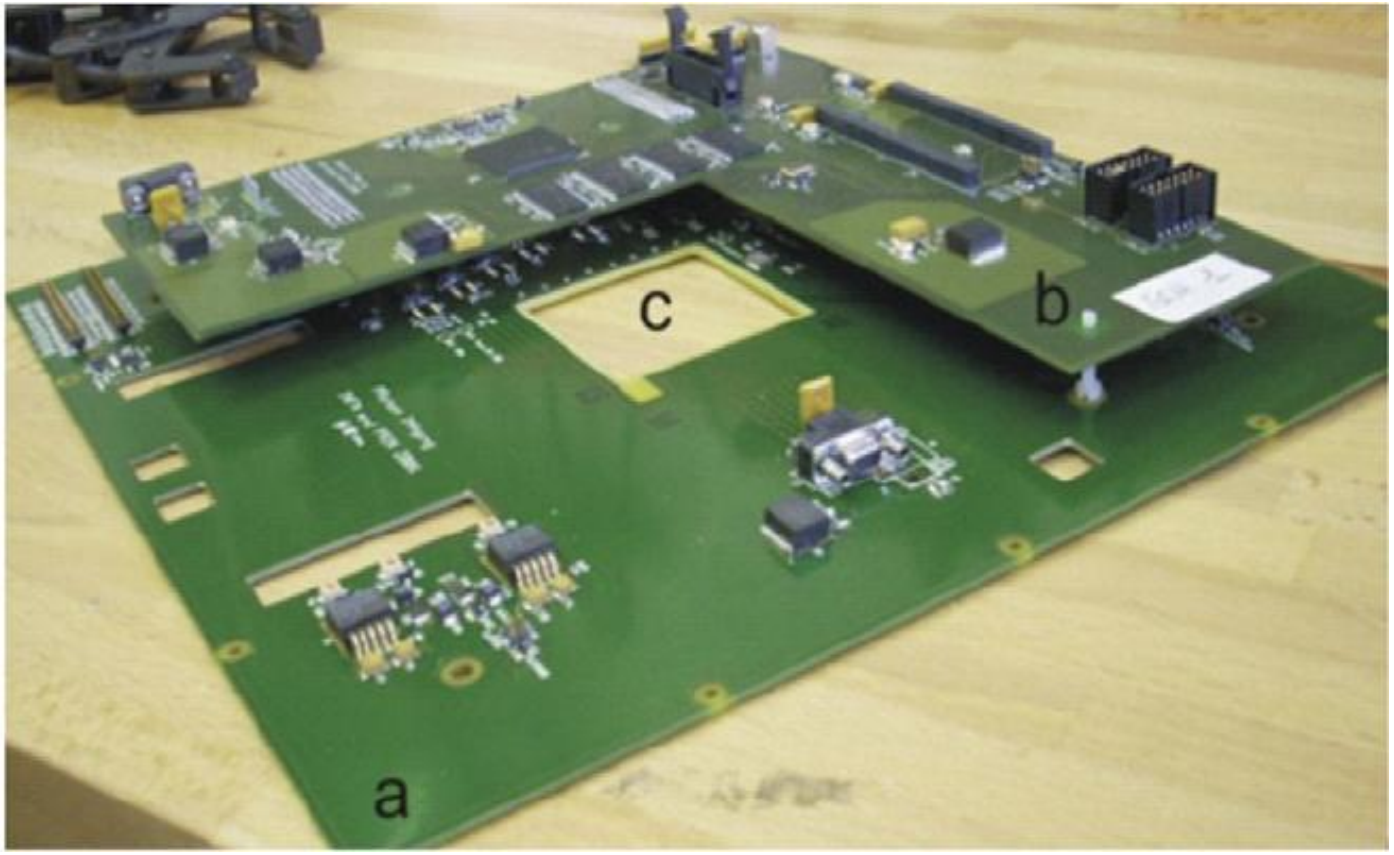
Cout suggested 47uF with ESR < = 200mΩ.



Cin ceramic (0.22 – 1)uF


Proton IMAging
INFN and PRIN 2006

FINAL BOARD



Front-end board (a); digital board (b); sensor slot (c).

C. Civinini, et al., Nucl. Instr. and Meth. A (2010), doi:10.1016/j.nima.2010.03.079