UNIVERSITÀ DEGLI STUDI FIRENZE
DINFO DIPARTIMENTO DI INGEGNERIA DELL'INFORMAZIONE

INGEGNERIA ELETTRONICA

Within the course of
ELETTRONICA DEI SISTEMI ANALOGICI E SENSORI
eSilicon will provide a Seminar titled

Introduction to DSP Based High Speed Serial Links

Date: 5th Nov 2019 | **Time:** 10.15am
Location: Aula Caminetto, Scuola Ingegneria

What you'll learn:

- What is a serial link
- Main challenges of high speed communication systems
- The "channel" at 50Gbit and above
- CMOS transmitter, limitation, equalization and implementation
- Equalization techniques
- Concept of DSP based PAM4 communication system and main building blocks
- Clock recovery system and circuits
- Receiver analog building blocks, CTLE and high speed ADC
- The Overall System

About the speaker: Matteo Pisati: received the M.Sc. and the Ph.D. degrees in electrical engineering from the University of Pavia, Italy, in 2001 and 2005, respectively. During his Ph.D., he worked on CMOS analog circuits for Clock and Data Recovery applications. From 2005 to 2012 he was with ST-Microelectronics, working as analog designer in the High Speed Serial Interface group. From 2012 to 2017 he worked for Marvell Semiconductor as project leader of the DSP-based PAM4 SerDes project. He is now Senior Manager at eSilicon, where he is leading the development of the 56Gb/s Serdes project.

About eSilicon: eSilicon provides complex FinFET ASICs, market-specific IP platforms and advanced 2.5D packaging solutions. Our ASIC-proven, differentiating IP includes highly configurable 7nm 56G/112G SerDes plus networking-optimized 16/14/7nm FinFET IP platforms featuring HBM2 PHY, TCAM, specialized memory compilers and I/O libraries. Our neuASIC™ platform provides AI-specific IP and a modular design methodology to create adaptable, highly efficient AI ASICs. eSilicon serves the high-bandwidth networking, high-performance computing, artificial intelligence (AI) and 5G infrastructure markets. www.esilicon.com

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